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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,366	KHAN ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,18-22,40,43-46,60,63,65,67-70,72 and 74-87* is/are pending in the application.

4a) Of the above claim(s) *40 and 43-46* is/are withdrawn from consideration.

5)☐ Claim(s) *14,18-22,60,63,65,67-70,72 and 74-87* is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 14, 18-22, 60, 63, 65, 67-70, 72 and 74-87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakashima et al. (US Pat. 5717252) in view of Higgins, III (US Pat. 5583377), Higgins III (US Pat. 5291062) and Karnezos (US Pat. 6020637).

Regarding claim 14, Nakashima et al. disclose a ball grid (BGA) package/apparatus (Fig. 21) comprising:

- a substrate such as an insulating tape/tape automated bonding (TAB) substrate (2 in Fig. 21; Col. 14, line 50) having a first/top and a second surface/bottom
- a metal plate/substrate/stiffener (4 in Fig. 21; Col. 15, line 64) having a first/top and a second/bottom surface, the metal substrate/stiffener providing enhanced support and strengthening/stiffening functions and improved reliability for the package/apparatus (Col. 5, line 5, Col. 6, line 44)

- a portion of the second/bottom surface of the metal plate/stiffener being attached to the first/top surface of the substrate/TAB substrate and substantially covering the first/top surface (see Fig. 21), wherein the metal plate/stiffener has a plurality of openings/holes formed there through (21a in Fig. 21; Col. 14, line 62) that are each open at the first/top and second/bottom surfaces
- an integrated circuit (IC) die (3 in Fig. 21) being mounted on the first/top surface of the metal plate/stiffener
- a plurality of solder balls (5 in Fig. 21; Col. 14, line 52) being attached to the second/bottom surface of the substrate/TAB substrate
- the substrate/TAB substrate having a window opening (not numerically referenced- see the central opening in 2 in Fig. 21)
- the metal substrate/stiffener having a centrally located cavity shaped portion protruding through the window opening of the substrate/TAB substrate such that a portion of the second/bottom surface of the metal plate/stiffener is exposed (see a central portion of 4 with respect to the opening in 2 in Fig. 21; Col. 15, line 67), and
- a plurality of wire bonds (see a bonding wire 7 for the respective opening 21a in Fig. 21) being attached to the IC die and to the first/top surface of the substrate/TAB substrate through the plurality of openings

(Fig. 21; Col. 15, line 61- Col. 16, line 5; Col. 14, line 14- Col. 15, line 8).

Nakashima et al. fail to teach:

a) the exposed portion of the second surface of the stiffener being configured to be mounted to a printed circuit board (PCB) to form an electrical and thermal path to the PCB, whereby heat is conducted over the thermal path from the IC die to the PCB during operation of the IC die, and

b) at least one wire bond that that couples at least one bond pad on a surface of the IC die to said first surface of the stiffener.

a) Higgins, III ('377 patent) teaches an exposed portion of a heat sink/stiffener being configured to be coupled/bonded to a user/external substrate (22 and 34 in Fig. 1 respectively; Col. 4, line 65). Higgins, III further teaches the exposed surface of the cavity portion of the heat sink/stiffener being coupled/bonded using a solder/plating (36 in Fig. 1) to a soldering pad (35 in Fig. 1) on the user/external substrate (34 in Fig. 1) to improve thermal conduction whereby heat is conducted over the thermal path from the IC die to the external substrate during operation of the IC die (Col. 4, lines 56- 67).

Higgins, III ('062 patent) teaches using a conventional mounting substrate such as a board/PCB for providing next level/external connections for a BGA package (Col. 4, line 25-30; Col. 5, line 55).

b) Karnezos teaches a BGA package having a bonding wire configuration such that an IC having a plurality of bonding wires (12 and 2626'/26" in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) is coupled to a stiffener/heat spreader (10 in Fig. 2) where a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) as taught by Higgins, III ('377 and '062 patents) and Karnezos respectively so that an external connection capability, interconnect density, power/ground routing and thermal dissipation can be improved in Nakashima et al's BGA package.

Regarding claim 18, Nakashima et al, Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 14 above, wherein Nakashima et al. teach the metal substrate/stiffener having the centrally located cavity shaped portion protruding through the window opening of the substrate/TAB substrate such that the cavity shaped portion forms the exposed of the second/bottom surface of the metal substrate/stiffener.

Regarding claim 19, Nakashima et al, Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claims 14 and 18 above, except the surface of the cavity portion being plated with the solder that allows the stiffener to be surface mounted to at least one soldering pad on the PCB.

Higgins, III ('377 patent) further teaches the exposed surface of the cavity portion of the heat sink/stiffener being coupled/bonded using a solder/plating (36 in Fig. 1) to a soldering pad (35 in Fig. 1) on the user/external substrate (34 in Fig. 1) to improve thermal conduction (Col. 4, lines 56- 67).

Higgins, III ('062 patent) teaches using a conventional mounting substrate such as a board/PCB for providing next level/external connections for a BGA package (Col. 4, line 25-30; Col. 5, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the surface of the cavity portion being plated with the solder that allows the stiffener to be surface mounted to at least one soldering pad on the PCB as taught by Higgins, III ('377 and '062 patents) so that the thermal conduction, bonding strength and the external connection capability can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA.

Regarding claim 20, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 14 above, except the stiffener being coupled to a first potential.

Higgins, III ('377 patent) further teaches the stiffener/heat sink being electrically coupled to a ground/first potential/voltage plane to achieve the desired grounding/voltage connection in addition to the thermal dissipation (Col. 9, lines 1-10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stiffener being coupled to a first potential as taught by Higgins, III ('377 patent) so that the desired grounding and voltage connection can be achieved and the thermal conduction can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA.

Regarding claim 21, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claims 14 and 20 above, except the IC die having a surface including at least one bond pad being a ground potential pad whereby stiffener operates as a ground potential plane.

Karnezos further teaches the BGA package where an IC having a plurality of bonding wires (12 and 2626'/26" in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) are coupled to a stiffener/heat spreader (10 in Fig. 2) such that a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC die having a surface including at least one bond pad being a ground potential pad whereby stiffener operates as a ground potential plane as taught by Karnezos so that the power/ground routing and thermal dissipation can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA package.

Regarding claim 22, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 14 above, wherein Nakashima et al. teach the substrate being the tape substrate.

Regarding claim 60, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 14 above, except the substrate being an organic substrate.

Higgins, III ('377 patent) further teach the substrate being made of a variety of conventional material including epoxy/organic/PCB, ceramic, etc. to provide the desired reinforcement and processing capability (Col. 3, line 43- Col. 4, line 7).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the organic substrate as taught by Higgins, III ('377 patent) so that the reinforcement, rigidity and thermal conduction can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA.

Regarding claim 80, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 14 above, wherein Nakashima et al. teach the metal plate/stiffener substantially covering the first surface of the substrate/TAB substrate (see Fig. 21).

Regarding claim 81, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claims 14 and 80 above, wherein the outer edges of the stiffener being substantially even with those of the substrate (see 4/2 in Fig. 21 of Nakashima et al. and 10/25 in Fig. 2 of Karnezos respectively).

Regarding claim 63, Nakashima et al. disclose a ball grid (BGA) package/apparatus (Fig. 21) comprising:

- a substrate such as an insulating tape/tape automated bonding (TAB) substrate (2 in Fig. 21; Col. 14, line 50) having a first/top and a second surface/bottom
- a metal plate/substrate/stiffener (4 in Fig. 21; Col. 15, line 64) having a first/top and a second/bottom surface, the metal substrate/stiffener providing enhanced support and strengthening/stiffening functions and improved reliability for the package/apparatus (Col. 5, line 5, Col. 6, line 44)

- a portion of the second/bottom surface of the metal plate/stiffener being attached to the first/top surface of the substrate/TAB substrate and substantially covering the first/top surface (see Fig. 21), wherein the metal plate/stiffener has a plurality of openings/holes formed there through (21a in Fig. 21; Col. 14, line 62) that are each open at the first/top and second/bottom surfaces
- an integrated circuit (IC) die (3 in Fig. 21) being mounted on the first/top surface of the metal plate/stiffener
- a plurality of solder balls (5 in Fig. 21; Col. 14, line 52) being attached to the second/bottom surface of the substrate/TAB substrate
- the substrate/TAB substrate having a window opening (not numerically referenced- see the central opening in 2 in Fig. 21)
- the metal substrate/stiffener having a centrally located cavity shaped portion protruding through the window opening of the substrate/TAB substrate such that a portion of the second/bottom surface of the metal plate/stiffener is exposed (see a central portion of 4 with respect to the opening in 2 in Fig. 21; Col. 15, line 67), and
- a plurality of wire bonds (see a bonding wire 7 for the respective opening 21a in Fig. 21) being attached to the IC die and to the first/top surface of the substrate/TAB substrate through the plurality of openings

(Fig. 21; Col. 15, line 61- Col. 16, line 5; Col. 14, line 14- Col. 15, line 8).

Nakashima et al. fail to teach:

a) the exposed portion of the second surface of the stiffener being configured to be mounted to a printed circuit board (PCB) to form an electrical and thermal path to the PCB, whereby heat is conducted over the thermal path from the IC die to the PCB during operation of the IC die, and

b) at least one wire bond that that couples at least one bond pad on a surface of the IC die to said first surface of the stiffener.

a) Higgins, III ('377 patent) teaches an exposed portion of a heat sink/stiffener being configured to be coupled/bonded to a user/external substrate (22 and 34 in Fig. 1 respectively; Col. 4, line 65). Higgins, III further teaches the exposed surface of the cavity portion of the heat sink/stiffener being coupled/bonded using a solder/plating (36 in Fig. 1) to a soldering pad (35 in Fig. 1) on the user/external substrate (34 in Fig. 1) to improve thermal conduction whereby heat is conducted over the thermal path from the IC die to the external substrate during operation of the IC die (Col. 4, lines 56- 67).

Higgins, III ('062 patent) teaches using a conventional mounting substrate such as a board/PCB for providing next level/external connections for a BGA package (Col. 4, line 25-30; Col. 5, line 55).

b) Karnezos teaches a BGA package having a bonding wire configuration such that an IC having a plurality of bonding wires (12 and 2626'/26" in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) is coupled to a stiffener/heat spreader (10 in Fig. 2) where a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) as taught by Higgins, III ('377 and '062 patents) and Karnezos respectively so that an external connection capability, interconnect density, power/ground routing and thermal dissipation can be improved in Nakashima et al's BGA apparatus.

Regarding claim 65, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 63 above, except the stiffener being coupled to a first potential.

Higgins, III ('377 patent) further teaches a stiffener/heat sink being electrically coupled to a ground/first potential/voltage plane to achieve the desired grounding/voltage connection in addition to the thermal dissipation (Col. 9, lines 1-10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stiffener being coupled to a first potential as taught by Higgins, III so that the desired grounding and voltage connection can be achieved and the thermal conduction can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's apparatus.

Regarding claim 67, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 63 above, wherein Nakashima et al. teach the IC die (3 in Fig. 21) being mounted on the first/top surface of the metal plate/stiffener in the cavity shaped portion of the metal plate/stiffener.

Regarding claims 68 and 69, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 63 above, except the IC die having a surface including a ground or a power signal pad so that the stiffener operates as a ground or power plane respectively.

Karnezos teaches a BGA package where an IC having a plurality of bonding wires (12 and 2626'/26" in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) are coupled to a stiffener/heat spreader (10 in Fig. 2) such that a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide

the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC die having a surface including a ground or power signal pad and a wire bond coupling the ground or power signal pad to the first surface of the stiffener respectively as taught by Karnezos so that the power/ground routing and thermal dissipation can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA apparatus.

Regarding claim 82, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 63 above, wherein Nakashima et al., teach the second surface of the metal plate/stiffener substantially covering the first surface of the substrate/TAB substrate to which the metal plate/stiffener is attached (Fig. 21).

Regarding claim 83, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claims 70 and 82 above, wherein the outer edges of the stiffener being substantially even with those of the substrate (see 4/2 in Fig. 21 of Nakashima et al. and 10/25 in Fig. 2 of Karnezos respectively).

Regarding claim 70, Nakashima et al. disclose a ball grid (BGA) package (Fig. 21) comprising:

- a substrate such as an insulating tape/tape automated bonding (TAB) substrate (2 in Fig. 21; Col. 14, line 50) having a first/top and a second surface/bottom
- a metal plate/substrate/stiffener (4 in Fig. 21; Col. 15, line 64) having a first/top and a second/bottom surface, the metal substrate/stiffener providing enhanced support and strengthening/stiffening functions and an improved reliability (Col. 5, line 5, Col. 6, line 44)
- a portion of the second/bottom surface of the metal plate/stiffener being attached to the first/top surface of the substrate/TAB substrate and substantially covering the first/top surface of the substrate/TAB substrate (see Fig. 21), wherein the metal plate/stiffener has a plurality of openings/holes formed there through (21a in Fig. 21; Col. 14, line 62) that are each open at the first/top and second/bottom surfaces
- an integrated circuit (IC) die (3 in Fig. 21) being mounted on the first/top surface of the metal plate/stiffener
- a plurality of solder balls (5 in Fig. 21; Col. 14, line 52) being attached to the second/bottom surface of the substrate/TAB substrate

- the substrate/TAB substrate having a window/window--shaped opening (not numerically referenced- see the central opening in 2 in Fig. 21)
- the metal substrate/stiffener having a centrally located cavity shaped portion protruding through the window opening of the substrate/TAB substrate such that a portion of the second/bottom surface of the metal plate/stiffener is exposed (see a central portion of 4 with respect to the opening in 2 in Fig. 21; Col. 15, line 67), and
- a plurality of wire bonds (see the bonding wire 7 for respective hole 21a in Fig. 21; Col. 14, line 62) being attached to the IC die and to the first/top surface of the substrate/TAB substrate through the plurality of respective openings

(Fig. 21; Col. 15, line 61- Col. 16, line 5; Col. 14, line 14- Col. 15, line 8).

Nakashima et al. fail to teach:

a) the exposed portion of the second surface of the stiffener being configured to be mounted to a printed circuit board (PCB) to form an electrical and thermal path to the PCB, whereby heat is conducted over the thermal path from the IC die to the PCB during operation of the IC die, and

b) at least one wire bond that that couples at least one bond pad on a surface of the IC die to said first surface of the stiffener.

a) Higgins, III ('377 patent) teaches an exposed portion of a heat sink/stiffener being configured to be coupled/bonded to a user/external substrate (22 and 34 in Fig. 1 respectively; Col. 4, line 65). Higgins, III further teaches the exposed surface of the cavity portion of the heat sink/stiffener being coupled/bonded using a solder/plating (36 in Fig. 1) to a soldering pad (35 in Fig. 1) on the user/external substrate (34 in Fig. 1) to improve thermal conduction whereby heat is conducted over the thermal path from the IC die to the external substrate during operation of the IC die (Col. 4, lines 56- 67).

Higgins, III ('062 patent) teaches using a conventional mounting substrate such as a board/PCB for providing next level/external connections for a BGA package (Col. 4, line 25-30; Col. 5, line 55).

b) Karnezos teaches a BGA package having a bonding wire configuration such that an IC having a plurality of bonding wires (12 and 2626'/26" in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) is coupled to a stiffener/heat spreader (10 in Fig. 2) where a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) as taught by Higgins, III ('377 and '062 patents) and Karnezos respectively so that an external connection capability, interconnect density, power/ground routing and thermal dissipation can be improved in Nakashima et al's BGA package.

Regarding claim 72, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 70 above, except the stiffener being coupled to a first potential.

Higgins, III ('377 patent) further teaches a stiffener/heat sink being electrically coupled to a ground/first potential/voltage plane to achieve the desired grounding/voltage connection in addition to the thermal dissipation (Col. 9, lines 1-10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stiffener being coupled to a first potential as taught by Higgins, III so that the desired grounding and voltage connection can be achieved and the thermal conduction can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA.

Regarding claim 74, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 70 above, wherein

Nakashima et al., teach the IC die being mounted on the first/top surface of the metal plate/stiffener in the cavity shaped portion of the metal plate/stiffener (Fig. 21).

Regarding claims 75 and 76, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 70 above, except the IC die having a surface including a ground or a power signal pad and a wire bond coupling the ground or power signal pad to the first surface of the stiffener respectively.

Karnezos further teaches a BGA package where an IC having a plurality of bonding wires (12 and 26'/26" respectively in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) are coupled to a stiffener/heat spreader (10 in Fig. 2) such that a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC die having a surface including a ground or power signal pad and a wire bond coupling the ground or power signal pad to the first surface of the stiffener respectively as taught by Karnezos so that the power/ground

routing and thermal dissipation can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA.

Regarding claim 84, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 70 above, wherein Nakashima et al., teach the metal plate/stiffener substantially covering the surface of the substrate/TAB substrate to which the metal plate/stiffener is attached (Fig. 21).

Regarding claim 85, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claims 70 and 84 above, wherein the outer edges of the stiffener being substantially even with those of the substrate (see 4/2 in Fig. 21 of Nakashima et al. and 10/25 in Fig. 2 of Karnezos respectively).

Regarding claim 77, Nakashima et al. disclose a ball grid (BGA) package (Fig. 21) having a comprising:

- a BGA package substrate such as an insulating tape/tape automated bonding (TAB) substrate (2 in Fig. 21; Col. 14, line 50) having a first/top and a second surface/bottom

- a metal plate/substrate/stiffener (4 in Fig. 21; Col. 15, line 64) having a first/top and a second/bottom surface, the metal substrate/stiffener providing enhanced support and strengthening/stiffening functions and an improved reliability (Col. 5, line 5, Col. 6, line 44)
- a portion of the second/bottom surface of the metal plate/stiffener being attached to the first/top surface of the BGA package substrate/TAB substrate, and substantially covering the first/top surface of the BGA package substrate/TAB substrate (see Fig. 21), wherein the metal plate/stiffener has a plurality of openings/holes formed there through (21a in Fig. 21; Col. 14, line 62) that are each open at the first/top and second/bottom surfaces
- an integrated circuit (IC) die (3 in Fig. 21) being mounted on the first/top surface of the metal plate/stiffener
- a plurality of solder balls (5 in Fig. 21; Col. 14, line 52) attached to the second/bottom surface of the substrate/TAB substrate
- the BGA package substrate/TAB substrate having a window/window-shaped opening (not numerically referenced- see the central opening in 2 in Fig. 21)
- the metal substrate/stiffener having a centrally located cavity shaped portion protruding through the window opening of the BGA package substrate/TAB substrate such that a portion of the second/bottom surface of the metal plate/stiffener is exposed (see a central portion of 4 with respect to the opening in 2 in Fig. 21; Col. 15, line 67), and

- a plurality of wire bonds (see a bonding wire 7 for the respective opening 21a in Fig. 21) being attached to the IC die and to the first/top surface of the BGA package substrate/TAB substrate through the plurality of openings

(Fig. 21; Col. 15, line 61- Col. 16, line 5; Col. 14, line 14- Col. 15, line 8).

Nakashima et al. fail to teach:

a) the exposed portion of the second surface of the stiffener being configured to be mounted to a printed circuit board (PCB) to form an electrical and thermal path to the PCB, whereby heat is conducted over the thermal path from the IC die to the PCB during operation of the IC die, and

b) at least one wire bond that that couples at least one bond pad on a surface of the IC die to said first surface of the stiffener.

a) Higgins, III ('377 patent) teaches an exposed portion of a heat sink/stiffener being configured to be coupled/bonded to a user/external substrate (22 and 34 in Fig. 1 respectively; Col. 4, line 65). Higgins, III further teaches the exposed surface of the cavity portion of the heat sink/stiffener being coupled/bonded using a solder/plating (36 in Fig. 1) to a soldering pad (35 in Fig. 1) on the user/external substrate (34 in Fig. 1) to improve thermal conduction whereby heat is conducted over the thermal path from the IC die to the external substrate during operation of the IC die (Col. 4, lines 56- 67).

Higgins, III ('062 patent) teaches using a conventional mounting substrate such as a board/PCB for providing next level/external connections for a BGA package (Col. 4, line 25-30; Col. 5, line 55).

b) Karnezos teaches a BGA package having a bonding wire configuration such that an IC having a plurality of bonding wires (12 and 2626'/26" in Fig. 2) and die pads including power and ground pads (not numerically referenced in Fig. 2) is coupled to a stiffener/heat spreader (10 in Fig. 2) where a bonding wire corresponding to a ground ring connection on the first surface of the stiffener/heat spreader is coupled to respective die pad/ground pad (26"/21 in Fig. 2; Col. 2, line 30-40) while additional wire bonds (26' in Fig. 2) are being used to provide the desired signal/power connections for the corresponding die pads to the substrate (Col. 2, lines 17-52).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) as taught by Higgins, III ('377 and '062 patents) and Karnezos respectively so that an external connection capability, interconnect density, power/ground routing and thermal dissipation can be improved in Nakashima et al's BGA package.

Regarding claims 78 and 79, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 77 above,

except a portion of the second surface is plated with a metal comprising a solder material to facilitate an attachment to the PCB.

Higgins, III ('377 patent) teaches the exposed surface of the cavity portion of the heat sink/stiffener being coupled/bonded using a solder/plating (36 in Fig. 1) to a soldering pad (35 in Fig. 1) on the user/external substrate (34 in Fig. 1) to improve thermal conduction (Col. 4, lines 56- 67).

Higgins, III ('062 patent) teaches using a conventional mounting substrate such as a board/PCB for providing next level/external connections for a BGA package (Col. 4, line 25-30; Col. 5, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a portion of the second surface is plated with a metal comprising a solder material to facilitate an attachment to a PCB as taught by Higgins, III ('377 and '062 patents) so that the thermal conduction, bonding strength and the external connection capability can be improved in Higgins, III ('377 and '062 patents), Karnezos and Nakashima et al's BGA.

Regarding claim 86, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claim 77 above, wherein Nakashima et al. teach the second surface of the metal plate/stiffener substantially covering the first surface of the BGA substrate/TAB substrate to which the metal plate/stiffener is attached (Fig. 21).

Regarding claim 87, Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach substantially the entire claimed structure as applied to claims 77 and 86 above, wherein the outer edges of the stiffener being substantially even with those of the substrate (see 4/2 in Fig. 21 of Nakashima et al. and 10/25 in Fig. 2 of Karnezos respectively).

Response to Arguments

3. Applicant's arguments filed on 01-26-04 have been fully considered but they are not persuasive.

A. Applicant contends that a combination of Nakashima et al. and Higgins, III ('377 patent) does not teach forming the electrical and thermal path to the PCB as recited in the independent claims.

However, as explained in the above ground of rejection, Nakashima et al. is combined with Higgins, III ('377 and '062 patents) and Karnezos, where Higgins, III ('377 and '062 patents) teach the external connection of the stiffener/heat sink with the PCB and Karnezos teaches using the wire bonding structure having the bonding wire being connected to the stiffener so that the combination of Nakashima et al., Higgins, III ('377 and '062 patents) and Karnezos teach forming the electrical and thermal path to the PCB.

B. Applicant contends that heat sink/metal substrate in Nakashima et al. and Higgins, III ('377 patent) are incorporated into different type of packages.

However, the packages/structures in Nakashima et al. and Higgins, III ('377 patent) comprise the BGA type packages (see Fig. 21 and 1 respectively) as recited in the independent claims.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956

Nitin Parekh

NP

04-06-04

Primary Examiner